**IN THE CLAIMS:**

1. (Cancelled)

2. (Previously Presented) Variable gain amplifier for amplifying a radio frequency signal by using a field effect transistor (FET) for signal amplification, in which the field effect transistor for signal amplification is of dual gate type, and

a first gate terminal is connected to a radio frequency signal input terminal via a DC cut capacitor at an input side of said FET for amplification and via an input impedance matching circuit,

a drain terminal is connected to a radio frequency signal output terminal via an output impedance matching circuit and a DC cut capacitor at an output side of said FET for amplification;

wherein a source terminal, of a field effect transistor (FET) for bypassing an amplifier element, is connected at a junction of the input side capacitor and the input impedance matching circuit via a DC cut capacitor at a source side of said FET for amplifier bypassing, a drain terminal of the field effect transistor for amplifier bypassing is connected at a junction of the drain terminal of the field effect transistor for signal amplification and the output impedance matching circuit via a DC cut capacitor at drain side of said FET for bypassing;

wherein the drain terminal of said field effect transistor for input impedance correction is connected at a junction of the input impedance matching circuit and a DC cut capacitor at an input side of said FET for amplification, via a first FET side DC cut capacitor for correction and a first FET side resistor for correction,

wherein a source terminal of the field effect transistor for input impedance correction is connected to ground via a first FET side bypass capacitor for correction;

wherein a drain terminal of a field effect transistor for output impedance correction is connected at a junction of the drain terminal of the field effect transistor for signal amplification and the output impedance matching circuit

via a second FET side DC cut capacitor for correction and a second FET side resistor for correction,

wherein a source terminal of the field effect transistor for output impedance correction is connected to ground via a second FET side bypass capacitor for correction;

wherein each gate terminal of the field effect transistor for amplifier bypassing, the field effect transistor for input impedance correction, and the field effect transistor for output impedance correction is connected to ground via a respective resistor;

wherein each drain terminal and source terminal of the field effect transistor for amplifier bypassing, the field effect transistor for input impedance correction, and the field effect transistor for output impedance correction are connected to a first control voltage application terminal via a respective resistor;

wherein a source terminal of the field effect transistor for signal amplification is connected to a second gate terminal and a drain terminal of a field effect transistor for bias SW via an inductor, this source terminal is connected to ground via a capacitor; and

wherein a source terminal of the field effect transistor for bias SW is connected to ground via a self-bias resistor, and a gate terminal thereof is connected to a second control voltage application terminal via a gate bias resistor.

3. (Previously Presented) Variable gain amplifier of Claim 2, wherein a selected one of said field effect transistor for amplifier bypassing, said field effect transistor for input impedance correction, and the field effect transistor for output impedance correction comprises a plurality of transistors connected in series.

4. (Previously Presented) Variable gain amplifier for amplifying a radio frequency signal by using a field effect transistor for signal amplification,

wherein an amplifier bypass means comprising a field effect transistor for amplifier element bypassing is connected parallel to the field effect transistor for signal amplification,

wherein a field effect transistor for bias SW for controlling the operation of the transistor for signal amplification is connected to the source terminal side of the field effect transistor for signal amplification, and

wherein a second gate terminal of the field effect transistor for signal amplification is connected at a junction of the source terminal of the field effect transistor for bias SW and a self-bias resistor.

5. (Previously Presented) Variable gain amplifier for amplifying a radio frequency signal by using a field effect transistor for signal amplification,

wherein the field effect transistor for signal amplification is of dual gate type, a first gate terminal is connected to a radio frequency signal input terminal via a first DC cut capacitor and an input impedance matching circuit, and a drain terminal is connected to a radio frequency signal output terminal via an output impedance matching circuit and a second a DC cut capacitor;

wherein a source terminal of a field effect transistor for amplifier element bypassing, is connected at a junction of the first DC cut capacitor and the input impedance matching circuit via a third DC cut capacitor, and a drain terminal, of the field effect transistor for amplifier element bypassing, is connected at a junction of the drain terminal of the field effect transistor for signal amplification and the output impedance matching circuit via a fourth DC cut capacitor;

wherein each gate terminal of the field effect transistor for signal amplification and field effect transistor for amplifier element bypassing is connected to ground via a respective resistor, a source terminal of the field effect transistor for signal amplification is connected to a drain terminal of a field effect transistor for bias SW via an inductor, and said drain terminal is connected to ground via a capacitor;

wherein a second gate terminal of the field effect transistor for signal amplification and the source terminal of the field effect transistor for bias SW are mutually connected, and a self-bias resistor and a bypass capacitor are connected between the junction and ground;

wherein a gate terminal of the field effect transistor for bias SW is connected to a second control voltage application terminal via a gate bias resistor; and

wherein the drain terminal and the source terminal of the field effect transistor for amplifier element bypassing are connected to a first control voltage application terminal via a respective resistor.